WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

(a) a semiconductor chip having a first main surface,

(b) a first insulating film formed over said first main surface of said semiconductor chip,

(c) an embedded interconnection slot formed over said first insulating film main surface,

(d) a connecting hole provided in a bottom surface of said embedded interconnection slot, and connected to a lower conducting layer,

(e) a conducting barrier film formed over surface regions of the bottom surface and side surface of said embedded interconnection slot and said connecting hole,

(f) an embedded metal interconnection layer having copper as its main component embedded in said interconnection slot and in said connecting hole in which said conducting barrier film is formed,

(g) a cap insulating film formed so as to cover said embedded metal interconnection layer and the upper surface of said first insulating film, and

(h) an upper insulating film formed over said cap insulating film, wherein:

the concentration of components other than copper in said embedded metal interconnection layer in the finished semiconductor chip does not exceed 0.8At%.

2. A semiconductor integrated circuit device as defined in Claim 1, wherein said components other than copper including silicon as main impurities.

3. A semiconductor integrated circuit device as defined in Claim 1, wherein said components other than copper including oxygen as main impurities.

4. A semiconductor integrated circuit device as defined in Claim 1, wherein said components other than copper including sulfur as main impurities.

5. A semiconductor integrated circuit device as defined in Claim 1, wherein said components other than copper including silicon, oxygen or sulfur, or any combinations of these as main impurities.

6. A semiconductor integrated circuit device as defined in Claim 1, wherein the concentration of components other than copper does not exceed 0.2At%.

7. A semiconductor integrated circuit device as defined in Claim 1, wherein the concentration of components other than copper does not exceed 0.08At%.

8. A semiconductor integrated circuit device as defined in Claim 1, wherein the concentration of components other than copper does not exceed 0.05At%.

9. A semiconductor integrated circuit device as defined in Claim 1, wherein the concentration of components other than copper does not exceed 0.02At%.

10. A semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10nm.

11. A semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 5nm.

12. A semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 3nm.

13. A semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10nm.

14. A semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 5nm.

15. A semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 3nm.

16. A semiconductor integrated circuit device as defined in Claim 1, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 2nm, or there is no conducting barrier film.

17. A semiconductor integrated circuit device as defined in Claim 1, wherein the width of said embedded interconnection slot does not exceed 0.4μm.

18. A semiconductor integrated circuit device as defined in Claim 1, wherein the width of said embedded interconnection slot does not exceed 0.25μm.

19. A semiconductor integrated circuit device as defined in Claim 1, wherein the width of said embedded interconnection slot does not exceed 0.2μm.

Sub a1

20. A method of fabricating a semiconductor integrated circuit device comprising:

(a) a semiconductor chip having a first main surface,

(b) a first insulating film formed over said first main surface of said semiconductor substrate,

(c) an embedded interconnection slot formed over said first insulating film main surface,

(d) a connecting hole provided in a bottom surface of said embedded interconnection slot, and connected to a lower conducting layer,

(e) a conducting barrier film formed over surface region of the bottom surface and side surface of said embedded interconnection slot and said connecting hole,

(f) an embedded metal interconnection layer having copper as its main component embedded in said interconnection slot and in said connecting hole in which said conducting barrier film is formed, and

(g) a cap insulating film formed so as to cover said embedded metal interconnection layer and the upper surface of said first insulating film, wherein:

a1

the concentration of components other than copper in said embedded metal interconnection layer in the finished semiconductor chip does not exceed 0.8At%, and

the purity of copper in the metal film when an embedded metal film having copper as its principal component is formed to form said embedded metal interconnection layer, is not less than 99.999%.

21. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the purity of said copper is not less than 99.9999%.

22. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein said metal film is formed by sputtering using a target wherein the purity of copper is not less than 99.999%.

23. A method of fabricating a semiconductor integrated circuit device as defined in Claim 21, wherein said metal

film is formed by sputtering using a target wherein the purity of copper is not less than 99.9999%.

24. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein said metal film is first planarized by chemical mechanical polishing, and said first main surface of said semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming said cap insulating film.

Sub B2

25. A method of fabricating a semiconductor integrated circuit device as defined in Claim 24, wherein said gas atmosphere comprises hydrogen as its principal component element.

26. A method of fabricating a semiconductor integrated circuit device as defined in Claim 24, wherein said gas atmosphere also has a nitriding action.

27. A method of fabricating a semiconductor integrated circuit device as defined in Claim 26, wherein said gas atmosphere comprises ammonia as its principal component element.

28. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein said chemical

mechanical polishing for forming the embedded metal interconnection layer is performed by abrasive particle-free chemical mechanical polishing. B

Sub B3

29. A method of fabricating a semiconductor integrated circuit device as defined in Claim 28, wherein the proportion of abrasive particles in a slurry used for said abrasive particle-free chemical mechanical polishing, does not exceed 0.5% as a mass ratio.

30. A method of fabricating a semiconductor integrated circuit device as defined in Claim 28, wherein the proportion of abrasive particles in a slurry used for said abrasive particle-free chemical mechanical polishing, does not exceed 0.1% as a mass ratio.

31. A method of fabricating a semiconductor integrated circuit device as defined in Claim 28, wherein the proportion of abrasive particles in a slurry used for said abrasive particle-free chemical mechanical polishing, does not exceed 0.05% as a mass ratio.

32. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.2At%.

33. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.08At%.

34. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.05At%.

35. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the concentration of components other than copper does not exceed 0.02At%.

36. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10nm.

37. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thinnest part of said conducting barrier

film in the side walls of said embedded interconnection slot and said connecting hole is not more than 5nm.

38. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 3nm.

39. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10nm.

40. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 5nm.

41. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20 wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 3nm.

42. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the film thickness of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is not more than 2nm, or there is no conducting barrier film.

43. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the width of said embedded interconnection slot does not exceed 0.4μm.

44. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the width of said embedded interconnection slot does not exceed 0.25μm.

45. A method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the width of said embedded interconnection slot does not exceed 0.2μm.